**VERSION 1.1**

**ERRORS:**

1. IR/IRX -> EEPROM address lines are mixed up and not contiguous.
2. U2 has the wrong silk-screen label (should be 74HC132, not 74HC10)
3. CARRY\_CLR/CARRY\_SET disables CONST\_OE\_00, causes floating databus.
4. Accidentally changed the 74HC161’s (program counter) parallel input from the MAR output bus to the general address bus. This means MAR\_SEL must be asserted when doing any JMP microinstructions. Otherwise the program counter will load its own value, canceling out the JMP instruction.
5. There is a very low chance of the reset operation causing a crash on bootup, at least at lower clock frequencies. Haven’t confirmed it. But, I think this is caused by the RESET line from the supervisory circuit going high at a particular IRX value and clock phase. I’ve only seen this happen at low clock frequencies so far (under 100KHz when using the crystal clock bypass, J2).

**IMPROVEMENTS FOR NEXT VERSION:**

1. Change USB port direction to point up.
2. Debug header (J4) can be reduced in size or even removed entirely.
3. Take out U5F from the reset line for U9 (74HC4040). Replace with the unused U2D (74HC132). This would allow the 74HC4040 to be reset by both IRX\_CLR and the supervisory POR circuit. This should eliminate error 5.

**NOTES:**

* Internal frequencies are defined by the crystal speed divided by 6, one for each of the six phases. Thus (12MHz/6 = 2MHz).
* Board is fully operational and stable at the on-board 2MHz clock rate (12MHz crystal). Design is fully static to allow for stopping the clock entirely. Under testing, the computer remains running up to around 3.8MHz (~23MHz crystal).But, this may or may not be very stable.
  + I’d need to do more analysis to see what the actual maximum frequency is. But, for now, I’m going to say that **the internal clock shouldn’t exceed 3.3MHz** (20MHz crystal).
    - This is due to the EEPROM’s 150ns address decoding time. For the three safe phases that the EEPROM address decoding is afforded, each phase delay needs to be 50ns apart. 50ns \* 6 = 300ns. 1/300ns = ~3.333MHz.
    - That being said, it’s possible that part of -CLK\_P2 could be added to that calculation. For example, during -CLK\_P2, the instruction register latches, which is the final change made to the EEPROM addresses during that cycle. For the 74HC273, that event may be around ~45ns, which would leave a fractional value of -CLK\_P2’s time that could be added to the above calculation. This could put the true maximum frequency closer to 3.5 or 3.6MHz.
    - But, the effective difference between 3.3MHz and ~3.6MHz isn’t really worth it. The better move would be to use faster EEPROMs.
    - Under testing, the computer loses stability completely at around 4MHz internal clock (24MHz crystal). This makes sense as it would give the EEPROMs (even accounting for the possible “fractional cycle” mentioned above) less than 150ns to decode their address lines.
* Computer draws around 150mA (enabling status LEDs pushes it to 180mA). d
* When programming the microcode EEPROMs, make sure to account for error #1. The EEPROM programmer must take the address line mixup into account. Right now, I’m solving this in software for the EEPROM writer.
* Because of error #3, you can not write a zero value to a register/memory at the same time you use CARRY\_CLR/CARRY\_SET when nothing is writing to the databus. For example, the microcode instruction:

ALU\_EN | CARRY\_CLR

gives the impression that it will be latching a zero value to the accumulator. But, in fact, the databus is floating because CONST\_OE\_00 is excluded from enabling from CARRY\_CLR.

* **IMPORTANT**: If you want to use a 74HC541 in place for U27, U1 **MUST** be a 74HC**T**10. The inputs for U1 must be TTL logic compatible.

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**VERSION 1.0**

**ERRORS:**

1. U6 GND not routed
2. U30A – RAM/ROM selector will not work. Fatal
3. U27A – ZF detector will not work. Fatal
4. uC ICP can be removed. Won’t work without removing IR and IRX.

**IMPROVEMENTS FOR NEXT VERSION:**

1. Change USB power interface for molex.
2. CV generator 01 value unused.

**NOTES:**

No further testing can be done because of error 2 and 3. Board is unfixable. Figured out these problems *just after* I soldered the board together. Oops.